Lower Cost Satellite Communication - Designing Integrated Circuits to Withstand Space Radiation

Farouk Smith, Sias Mostert
Dept. of Electrical Engineering, University of Stellenbosch
Stellenbosch 7600, South Africa
{fsmith, mostert}@sun.ac.za

Abstract — **This research focuses on current issues in the literature with regards to the effect of radiation on the performance on Commercial of the Shelf (COTS) components in space. There is increasing use of commercial components in space technology and it is important to recognize that the space radiation environment poses particular problems. The integrated circuits used for spacecraft electronics must be resistant to radiation. Understanding how space radiation interacts with microelectronics is the first step in establishing ways to mitigate adverse effects. A specific methodology is needed to select and quantify the operation of COTS components in the space radiation environment. Therefore, the key objective of this research is to find a suit of design rules and strategies to achieve a significant lifetime in a GEO orbit through the use of COTS components. A novel design technique for hardening digital electronic circuits against Total Ionizing Dose (TID) and Single Event Upsets (SEU) has been introduced. The new method is termed Selective Time Division Modular Redundancy (STDMR) is currently being considered for a provisional international patent. Until the provisional patent is registered, only background information is provided.**

1. INTRODUCTION

The study of radiation effects on semiconductor devices started about forty years ago, when the first satellites experienced serious problems due to the detrimental effect on their electronic circuits as a result of space radiation. Since then, there has been an increasing interest in the study of circuits which can work in a radiation environment, driven by all the possible applications of these kinds of circuits, such as advanced weaponry, instrumentation for nuclear power plants, high-energy physics experiments and, last but not least space missions and satellites.

There is increasing use of commercial components in space technology and it is important to recognize that the space radiation environment poses particular risks [1]. In order to meet satellite mission requirements, spacecraft are more complex and the technologies that meet requirements are increasingly sensitive to environment effects and have responses that are difficult to quantify. An example of this is the demand for COTS electronics that reduces the availability of components hardened for space environments.

The objective of satellite communications is to achieve as much coverage area with as low a cost as possible and in order to reduce the cost of manufacturing a satellite, one could make use of COTS components. However, these COTS components are very susceptible to the hazards of the space environment.

The integrated circuits used for spacecraft electronics must be resistant to radiation [2, 3]. The need of radiation tolerant circuits for the various applications led in the past to the development of special technologies, called radiation hardened, where particular processing methods are used in order to improve their radiation tolerance. Modifying the process steps is one of the three ways to improve the radiation tolerance of an integrated circuit. The two other possibilities are to use special layout techniques or special circuit and system architectures [4, 5, 6].

The radiation hardened method would be to modify the manufacturing process of the IC's. For example, by reducing the oxide thickness in a MOS transistor, the device becomes less susceptible to TID degradation, because less charges can become trapped in the smaller oxide volume. However, with the shrinking device volume, it becomes more susceptible to Single Event Effects (SEE), due to a smaller particle energy being necessary to cause an upset.

The fabrication method or transistor design cannot be influenced by the system engineer, and to use radiation hard components would defeat the main objective of keeping the satellite cost as low as possible.

The second method involves the use of special layout techniques, which solved the problem of radiation induced leakage currents and Single Event Latchup (SEL) and reduce the vulnerability due to Single Event Upsets (SEU). A new radiation tolerant transistor structure can be obtained without any process fabrication modifications [7]. The NMOS transistor and field leakage normally induced by ionizing radiation can be remedied by acting on the work function of the transistor gate at the transistor edges. The technique also works in a CMOS process where transistor source and drains are silicided. It decreases device density that can be achieved with the technology and slows down digital circuits due to an increase in node capacitances. It was demonstrated that the functionality of the transistor structure and its radiation tolerance was intact up to 40 Mrad(SiO_2).

The third method in which to make CMOS IC's radiation tolerant is to use special circuit architectures that are less sensitive than others to the changes in the device characteristics due to radiation. Several methods can be employed to harden a circuit for TID induced effects. Modeling the radiation-induced variation as a function of the total dose of several transistor parameters, such as the trans-conductance and the threshold voltage, allow to foresee the drift of the circuit operating point, and therefore one can design the circuit in order to make it flexible enough to tolerate these drifts.

Another method, which falls into the third category, in which to make CMOS circuits tolerant to ionizing radiation is to distribute the workload among the various paths in the circuit. This new method is the focus of this research.

Understanding how space radiation interacts with microelectronics is the first step in establishing ways to mitigate adverse effects. Therefore, the impact of space radiation on digital electronics needs to be understood in order to design circuit architectures to increase the radiation robustness of systems in the space radiation environment.

The rest of this paper is structure as follows: Following a discussion of the effects of ionizing radiation on electronics in section 2, a brief overview of the MOS radiation response is given in section 3. Section 4 provides an introduction to SEE. A mathematical discussion of collusion cross section is provided in section 5, followed by a mathematical model to support the proposed STDMR method to mitigate for SEU in section 6. Section 7 concludes this paper.

2. TID EFFECTS ON ELECTRONIC COMPONENTS

The interaction of radiation with matter is a very broad and complex topic. In this section we try to analyze the problem with the aim of explaining the more important aspects, which are essential for a physical comprehension of the degradation observed in electronic devices and circuits under radiation.

The manner in which radiation interacts with solid materials depends on the type, kinetic energy, mass and charge of the incident particle and the mass, atomic number and density of the target material. The effects can be classified in the following three ways: 1) Total dose as a result of ionization damage, 2) Bulk effects as a result of displacement damage and 3) Single Event Effects as a result of an energetic particle strike [8, 9].

Ionizing radiation dose is defined as the amount of energy deposited by ionization per unit mass of material. SI Units are J/Kg (rad). The majority of radiation effects depend on rate of delivery and so dose-rate information is required. In particular, Total Ionizing Dose (TID) radiation induced charge buildup in MOS devices depends on: dose, dose rate, type of ionizing radiation, applied and internal electric fields, device geometry, operating temperature, post-irradiation conditions (e.g. time and temperature), dielectric material properties, fabrication processing, oxide impurities, nitrogen and sodium, final processing packaging, burn-in reliability screens, and aging [4]. Issues of IC architecture also impact survivability against TID effects.

Accumulated dose leads to threshold voltage shifts in CMOS devices due to trapped holes in the oxide and the formation of interface states. In addition increased leakage currents and gain degradation in bipolar devices can occur [10]. It has been shown that the dominant radiation effects in MOS devices are due to TID effects, and not due to displacement damage, the usual cause of radiation-induced degradation in bipolar devices [4].

To understand the operation of the metal-oxide semiconductor field effect transistor (MOSFET), which is the basic building block of modern digital circuits, refer to Fig. 1. The diagram illustrates the case of an n-channel using a p-type substrate. The normal operation of the NMOS transistor is as follows: When a positive voltage is applied to the gate terminal, an electric field is created between the gate and the silicon substrate.

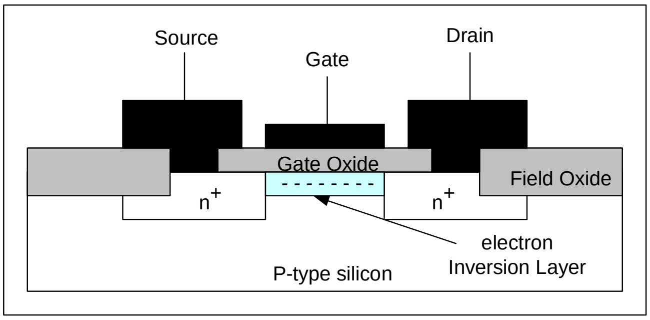

Fig. 1 Basic schematic of the MOS transistor

In effect, this behavior is very much the same as a parallel plate capacitor. Due to the presence of the electric field, the majority carriers in the substrate (holes in p-type) will be repelled from the gate-oxide substrate interface and minority carriers (electrons) will be attracted, forming what is termed an inversion layer. When a potential difference is applied between the source and drain terminals, the inversion layer provides a low resistance path for electrons to flow. The device is said to be turned on, and the gate voltage at which the inversion layer just begin to transmit current is termed the threshold voltage of the device.

The effect of using the MOSFET device in a radiation environment is that the gate oxide becomes ionized by the dose it absorbs due to the radiation induced trapped charges in the gate-oxide. The trapped charges in the gate-oxide generate additional space charge fields at the oxide-substrate interface. After a sufficient dose, a large positive charge builds up, having the same effect as if a positive voltage was applied to the gate terminal. Therefore, the transistor source to drain current can no longer be controlled by the gate terminal and the device remains on permanently resulting in device failure.

The radiation response of the PMOS transistor exhibits the same pattern, but the effect is opposite. The normal operation of the PMOS transistor is as follows: When a negative voltage is applied to the gate terminal with respect to the substrate, an electric field is also created between the gate and substrate. However, this field is in the opposite direction as in the case of NMOS. When exposed to ionizing radiation, the free electrons move in the direction of the silicon substrate, whereas the positive holes move in the direction of the gate oxide interface where they become trapped in impurity sites. This means that positive charge buildup in PMOS devices is less severe than in NMOS, because the charges get trapped at the gate oxide interface. Thus, the charge buildup in PMOS devices is less effective in shifting the threshold voltage of the device [11]. Already it should be clear that the direction of the electric field in the gate oxide has a major effect on the radiation response of the device.

Conceptually, the radiation induced oxide charge buildup problems is a simple principle. It is only when one tries to quantify the details of the radiation response that one realizes the complexities involved in the radiation response of the MOS transistor. For example, the radiation response of a MOS transistor has a very complex time-dependant response which is not only important to understand the physics of the response, but also for the practical issues of testing, predicting and hardness assurance [12].

3. OVERVIEW OF THE MOS RADIATION RESPONSE

The MOS radiation response involves several different processes [13]. Each of these processes depends on time, temperature, applied field, process history, etc. as mentioned in the previous section. A basic illustration of the overall radiation response of the MOS transistor is shown in Fig. 2.

In Fig. 2 a positive bias voltage is applied to the gate terminal as in the case of NMOS. When ionizing radiation strikes the gate oxide, electrons are freed from the oxide molecules and are swept by the direction of the electric field towards the gate terminal. The free holes move in the direction of the substrate.

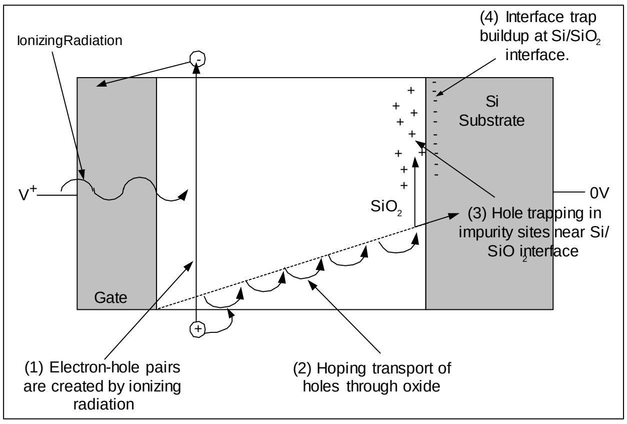

Fig. 2 The basic radiation effects in MOS transistors

The four main processes involved in the radiation response of MOS devices are illustrated in Fig.2. First, the ionizing radiation acts with the gate oxide layer to produce electron-hole pairs [12, 13]. Some fraction of the electron-hole pairs recombine depending on the type of incident particle and the applied gate to substrate voltage, i.e. the electric field. The mass of the electron is much less than the mass of the hole, and is swept away very quickly in the direction of the gate terminal. The time for the electrons to be swept away is on the order of 1 ps [13]. The much heavier holes that escape recombination remain near their point of origin. The number of these surviving holes determine the initial response of the device after a short pulse of radiation. The cause of the first process is the main motivation for design method described in the next section. The other processes will only be described briefly below. For a full review of these processes the reader is referred to [12, 13, 14, 15].

The second process in Fig. 2 is the slow transport of holes toward the oxide-silicon interface due to the presence of the electric field. It is this transport that explains the short term recovery of MOS devices [12]. When the holes reach the interface, process 3, they become trapped in impurity sites and this is the main cause of the permanent threshold voltage shift in MOS devices.

The fourth process is the buildup of interface states in the substrate near the interface. A negative space charge region is created near the interface because of the positive charge buildup of process 3.

4. SEE EFFECTS ON ELECTRONIC COMPONENTS

Single Event Effects (SEE) are caused by ionization, as a consequence of the impact of a heavy ion (cosmic ray) or proton. The ionization induces a current pulse in a p-n junction. SEE covers both Single Event Upset (SEU), or ‘soft error’, and Single Event Latch-up (SEL). Fig. 3 illustrates how an energetic particle can produce a spurious electrical signal. The particle produces charges along its path, in the form of electrons and holes. These are collected at the source and drain, and a current pulse appears. This can be large enough to produce an effect like that of a normal signal applied to the transistor.

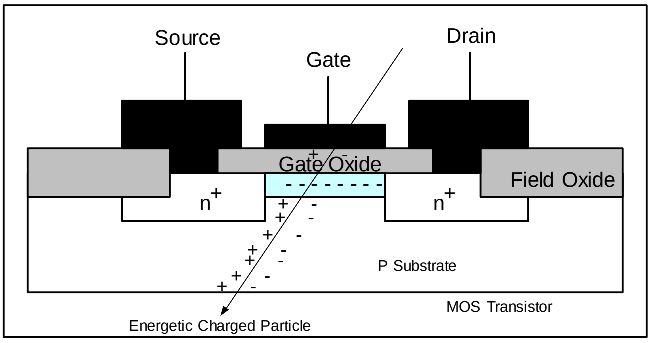

Fig.3 SEE Energetic particle strike

In the case of SEU, the current pulse may non-destructively change the state of a bi-stable element. In a satellite computer, for example, a bit-flip could randomly change critical data, randomly change the program, or confuse the processor to the point that it crashes.

For a SEU particle strike to result in a soft error in a combinational circuit, three conditions have to be satisfied: (1) an active path must exist between the afflicted node and the output of the circuit. (2) The pulse must be wide enough to avoid inertial delay filtration through subsequent gates, and survive electrical attenuation along the active path. Finally (3), the pulse should arrive within the setup and hold time of a latch element to be captured and cause a soft fault [16, 17].

The proposed design technique in this research concentrates on the first condition, and specifically on the role of the active path in the propagation of the SEU through the circuit. The active state of a gate along the SEU path to an output can inhibit the upset propagation. The nature of particle-induced upsets is a probabilistic one, and if a device is large it presents a greater target for energetic particle strikes.

The most common method to mitigate for SEU is to use redundant information storage or error-checking circuitry. For example, a widely used technique know as Triple Modular Redundancy (TMR) is a design hardening technique for obtaining high immunity against SEU. With this technique, a single latch does not affect a change in bit state, but rather three identical latches are queried, and the state will only change if the majority of latches are in agreement. Thus, a single latch error will be voted away by the others [18, 19].

Another method that makes use of redundancy to mitigate for SEU, is called Selective TMR [19]. Instead of providing redundancy for each gate as in the case of TMR, STMR identifies SEU sensitive gates in the circuit and only provides redundancy for those gates.

The main disadvantage of TMR is the excessive area overhead. The hardened design has 200% more area than the original circuit. STMR provides better utilization of system resources than TMR [19]. As far as system power is concerned, TMR also uses 200% more power than the original circuit. STMR also has a considerable power consumption overhead, although less than TMR. The excessive power utilization in TMR and STMR is because all three redundant gates are simultaneously active, thereby consuming three times as much power as the original gates.

The method proposed in this research, called Selective Time Division Modular Redundancy (STDMR), uses the same amount of power as the original circuit, and simultaneously provides mitigation for both SEE and Total Ionizing Dose (TID). This dual mitigation feature makes it the only known method to cater for both SEE and TID simultaneously, as well as saving system power compared to TMR and STMR.

The motivation for STDMR as far as its SEU mitigation capability is concerned, is provided by means of a mathematical model of particle collision. The methodology and concepts are well known techniques in nuclear physics.

5. DEFINITION OF COLLISION CROSS SECTION

The interaction or collision between two particles is usually described in terms of the cross section [20, 21], which is defined as: ‘A measure of the probability that an encounter between particles will result in the occurrence of a particular event or reaction. Also called collision cross section’ [21]. This parameter is basically a measure of the effectiveness of the projectile– target interaction. The larger the cross section, the more likely it is that the projectile particles interacts with its target. Cross section has the dimension of area and represents the effective area of the region of the collision [21, 22, 23]. A cross section depends on the types of particles involved and usually depends on the velocity or energy of the projectile particles.

The formal definition of microscopic cross section is given as follows [21]. Consider a beam of particles with intensity $\mathbf{I_0}$, incident upon a target of density ρ, i.e. particles per unit area, as shown in Fig. 4. Now look at the number of particles absorbed or scattered by the target, $\mathbf{I_s}$.

Because of the randomness of the impact parameter, which is the distance between the projectile and a target particle, the number of scattered projectiles will fluctuate over different measurements. However, if one averages many measurements, this number will tend towards a fixed amount. The cross section, σ , is then defined as

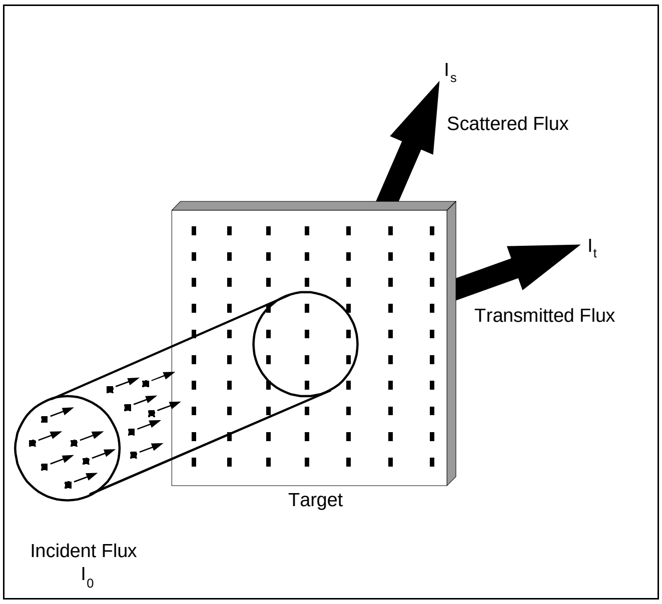

Fig. 4 A beam of particles are partially scattered by a target.

$$\sigma = \frac{I_s}{\rho I_0} \quad (1)$$

Hence, σ is the average fraction of scattered projectiles divided by the number of target particles per unit area. Equation (1) says that if the number of particles present in the target, ρ, increases, so does the number of collisions, $\mathbf{I_s}$, given that the cross section is a fixed number. One must divide by this factor if the cross section is to represent the effective area of interaction between a single beam particle and a target.

We now describe a method using equation (1), which is based on the measurement of the growth of the number of scattered projectiles as a function of the target density ρ. Equation (1) can be rewritten as

$$\frac{I_s}{I_0} = \sigma\rho \quad (2)$$

The above equation says that the fraction of scattered projectiles, I_s/I_0, depends linearly on the target density. Therefore, the measurement of the cross sections can be reduced to the study of the dependence of the growth rate of the scattered projectiles on the target density. Consequently, the cross section can be determined from the linear part of the growth rate of the scattered projectiles, i.e. from the slope in the plot of I_s/I_0 versus ρ.

The same procedure is used when performing a SEE test on a device. The device under test (DUT) is monitored while it is being irradiated with energetic particles. By counting the number of SEU’s and knowing how many particles passed through the part (with particle counter), we can calculate the likelihood of a particular particle causing a SEU. This resultant number, which is the number of upsets divided by the number of particles per cm^2 causing the upsets, is called the cross-section of the part and is measured in units of cm^2/ device.

6. THE PROPSED MODEL FOR SEE

In order to simplify the development of the model, it is assumed that a soft error hit on a gate as a whole will result in an error, as opposed to considering individual nodes, which is more realistic. This is illustrated in Fig. 5.

We use the theory of the previous section as follows:

In the formal definition of cross section as defined in the previous section, the target density ρ, is the no. of particles per unit area. In order to be able to use this concept in our description of SEE, another requirement has to be satisfied.

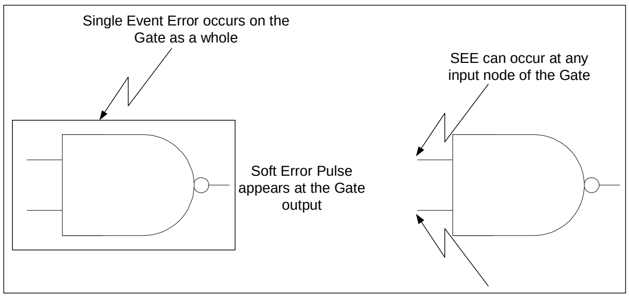

Fig.5 SEE occurring at a Gate or an individual node

First, we consider a gate as a whole to be the target particle. However, from the introduction, a necessary condition for the projectile particle to cause a SEE, **an active path must exist** between the afflicted node and the output of the circuit. The "activity" of a given node or gate is basically its frequency of use in a circuit. For example, if the gate is struck by an energetic particle, but at that moment is inactive in the circuit, it will not result in a SEE. Thus we have to relate the density (as defined in the previous section), to the gates frequency of use in the circuit.

A natural consequence of this is that the density is not only dependant on the physical arrangement of the target gates, but also whether it is in use when it gets struck by an energetic particle.

We now define a new density, which we call the SEE density, denoted by ρ_{SEE} . ρ_{SEE} is some fraction or function of the total number of gates in the circuit (ρ), depending on the average frequency of use of all the gates in the circuit ($F_{use,ave}$). $F_{use,ave}$ in turn is a function of the processor clock frequency, f_c, and the specific system application. Thus,

$$\rho_{\text{SEE}} = Function(\rho, f_c, application) \qquad (3)$$

ρ_{SEE} is the average amount of gates per unit area available for SEE.

The clock frequency, f_c, is essentially the smallest time interval between an active and inactive state of a circuit gate. It is important to note that the faster f_c and $F_{use,ave}$, the more often the gate is in the active state, and therefore is more susceptible to SEE.

Thus,

$$\rho_{SEE} \rightarrow \rho_{Total} \qquad (4)$$

as f_c and $F_{use,ave}$ increase.

If we now substitute equation 3 into equation 1, we have for the SEE cross section, σ_{SEE} ,

$$\sigma_{SEE} = \frac{I_{SEE}}{Funtion(\rho, f_c, application) I_0} \qquad (5)$$

The severity of a radiation environment is usually expressed as an integral linear energy transfer spectrum, which gives the flux of particles depositing more than a certain amount of energy (and hence charge) per unit path-length of material. Energy deposited per unit path-length is referred to as linear energy transfer (LET) and the common units are MeV per g cm$_{-2}$ or per mg cm$_{-2}$. Devices are characterized in terms of a cross-section (effective area presented to the beam for a SEE to occur), which is a function of LET. For each device there is a threshold LET below which SEE does not occur.

According to the literature, the vulnerability of a device to Single Event Effects is defined by two parameters [24, 2]:
Saturated Cross-Section. This is when all incident ions are capable of producing an effect and no increase is seen in the event rate for an increase in LET. The cross-section has the dimensions of cm2 and, for SEU is a function of the surface area of the sensitive nodes.
Threshold LET. This is the minimum LET required to produce SEE and is generally defined as the LET at which the cross-section is 10% of the saturated cross-section.

However, as can be deduced from equation 5, the sensitivity of a device to SEE should also include the transistor packing density, the system or clock frequency, and the intended system application. As device sizes shrink the threshold LET is becoming lower and SEE rates are increasing [18].

7. CONCLUSIONS

We proposed a new design technique for TID and SEE mitigation in digital electronic circuits. The method consists of selectively applying Time Division Modular Redundancy to critical modules in the circuit. The new method is termed Selective Time Division Modular Redundancy (STDMR) is currently being considered for a provisional international patent. Until the provisional patent is registered, only background information is provided. It was shown with a mathematical model of the collision cross section, that the sensitivity of a device to SEE includes the transistor packing density, the system or clock frequency, and the intended system application. The dual mitigation feature of STDMR makes it the only known method to cater for both SEE and TID simultaneously, as well as saving system power compared to TMR and STMR.

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