Reconfigurable computing for TID Mitigation in Digital Satellite Circuits

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Abstract — **We present a novel design technique for hardening digital electronic circuits against Total Ionizing Dose (TID). There is increasing use of commercial components in space technology and it is important to recognize that the space radiation environment poses particular risks. The integrated circuits used for spacecraft electronics must be resistant to radiation. The amount of threshold voltage shift in MOS devices caused by ionizing radiation is strongly dependant on the bias voltage applied to the gate terminal during radiation. The threshold voltage shift is much less severe under the influence of ionizing radiation if the gate voltage is 0V with respect to the device substrate. We have direct control of the bias voltage applied to the gate terminal, and therefore can control the rate of threshold voltage shift in the MOS device. Digital electronic circuits can be hardened against TID effects by selectively applying Modular Redundancy. Double Modular redundancy is applied, activating one while the other is inactivated, thereby allowing the modules to anneal during its "off" cycle. The new design technique provides greatly improved TID tolerance.**

1. Introduction

The study of radiation effects on semiconductor devices started about forty years ago, when the first satellites experienced serious problems due to the detrimental effect on their electronic circuits as a result of space radiation. Since then, there has been an increasing interest in the study of circuits which can work in a radiation environment, driven by all the possible applications of these kinds of circuits, such as advanced weaponry, instrumentation for nuclear power plants, high-energy physics experiments and, last but not least space missions and satellites.

The objective of satellite communications is to achieve as much coverage area with as low a cost as possible and in order to reduce the cost of manufacturing a satellite, one could make use of COTS components. However, these COTS components are very susceptible to the hazards of the space environment.

The need of radiation tolerant circuits for the various applications led in the past to the development of special technologies, called radiation hardened, where particular processing methods are used in order to improve their radiation tolerance. Modifying the process steps is one of the three ways to improve the radiation tolerance of an integrated circuit. The two other possibilities are to use special layout techniques or special circuit and system architectures [1- 3].

Another method, in which to make CMOS circuits tolerant to ionizing radiation is to distribute the workload among redundant modules in the circuit. This new method will be described in detail in the sections that follow.

Several studies have been done that considers the effect of the gate bias on the radiation response of MOS oxides [4 - 7]. The general conclusion of these studies were that the amount of threshold shift in MOS devices caused by ionizing radiation is strongly dependant on the bias voltage applied to the gate both during and after radiation. Further, it has been reported that the trapped positive charge near the oxide-silicon interface anneal quickly when irradiated in an unbiased condition [4]. The research by [4] showed that the effect of alternating bias on the radiation response of MOS devices were a reduced amount of hole trapping and interface state buildup in N-channel devices. In P-channel devices a reduced amount of hole trapping were also evident. Thus, for devices which are subject to gate bias cycling, the maximum acceptable dose is higher than if the irradiation bias were applied continuously. By adding redundancy and applying a resting policy, one can significantly prolong the useful life of MOS components in space.

The main focus of this paper is to apply this resting policy to mitigate for Total Ionizing Dose (TID) effects in FPGA's. Fundamentally the radiation effects of FPGA's are not any different from any other CMOS-based digital IC [8]. Each FPGA is unique in its architecture, and each has its unique response to radiation. However, the issue is to correlate the radiation induced response to the basic mechanisms of the MOS radiation response.

The rest of this paper is structure as follows: Following a discussion of the effects of ionizing radiation on electronics in section 2, a brief overview of the MOS radiation response is given in section 3. In section 4, a brief description of the FPGA TID response is given. Section 5 provides a detailed description of the proposed SMR design method. The method in which to apply the SMR method in FPGAs is discussed in section 6. Section 7 provides experimental results and section 8 concludes this paper.

2. Effects On Electronic Components

The interaction of radiation with matter is a very broad and complex topic. In this section we try to analyze the problem with the aim of explaining the more important aspects, which are essential for a physical comprehension of the degradation observed in electronic devices and circuits under radiation.

The manner in which radiation interacts with solid materials depends on the type, kinetic energy, mass and charge of the incident particle and the mass, atomic number and density of the target material. The effects can be classified in the following three ways: 1) Total dose as a result of ionization damage, 2) Bulk effects as a result of displacement damage and 3) Single Event Effects as a result of an energetic particle strike [9, 10]. In this paper we concentrate on the design techniques to mitigate TID effects, and therefore only discuss the effects due to ionizing radiation.

Ionizing radiation dose is defined as the amount of energy deposited by ionization per unit mass of material. The majority of radiation effects depend on rate of delivery and so dose-rate information is required. In particular, Total Ionizing Dose (TID) radiation induced charge buildup in MOS devices depends on: dose, dose rate, type of ionizing radiation, applied and internal electric fields, device geometry, operating temperature, post-irradiation conditions (e.g. time and temperature), dielectric material properties, fabrication processing, oxide impurities, nitrogen and sodium, final processing packaging, burn-in reliability screens, and aging [1]. Issues of IC architecture also impact survivability against TID effects.

Accumulated dose leads to threshold voltage shifts in CMOS devices due to trapped holes in the oxide and the formation of interface states. In addition increased leakage currents and gain degradation in bipolar devices can occur [10]. It has been shown that the dominant radiation effects in MOS devices are due to TID effects, and not due to displacement damage, the usual cause of radiation-induced degradation in bipolar devices [1].

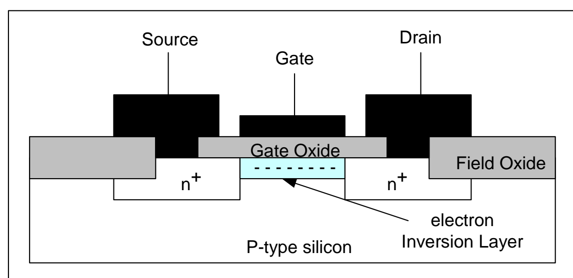

Fig. 1 Basic schematic of the MOS transistor

To understand the operation of the metal-oxide semiconductor field effect transistor (MOSFET), which is the basic building block of modern digital circuits, refer to Fig. 1. The diagram illustrates the case of an n-channel using a p-type substrate. The normal operation of the NMOS transistor is as follows: When a positive voltage is applied to the gate terminal, an electric field is created between the gate and the silicon substrate. In effect, this behavior is very much the same as a parallel plate capacitor. Due to the presence of the electric field, the majority carriers in the substrate (holes in p-type) will be repelled from the gate-oxide substrate interface and minority carriers (electrons) will be attracted, forming what is termed an inversion layer. When a potential difference is applied between the source and drain terminals, the inversion layer provides a low resistance path for electrons to flow. The device is said to be turned on, and the gate voltage at which the inversion layer just begin to transmit current is termed the threshold voltage of the device.

The effect of using the MOSFET device in a radiation environment is that the gate oxide becomes ionized by the dose it absorbs due to the radiation induced trapped charges in the gate-oxide. The trapped charges in the gate-oxide generate additional space charge fields at the oxide-substrate interface. After a sufficient dose, a large positive charge builds up, having the same effect as if a positive voltage was applied to the gate terminal. Therefore, the transistor source to drain current can no longer be controlled by the gate terminal and the device remains on permanently resulting in device failure.

The radiation response of the PMOS transistor exhibits the same pattern, but the effect is opposite. The normal operation of the PMOS transistor is as follows: When a negative voltage is applied to the gate terminal with respect to the substrate, an electric field is also created between the gate and substrate. However, this field is in the opposite direction as in the case of NMOS. When exposed to ionizing radiation, the free electrons move in the direction of the silicon substrate, whereas the positive holes move in the direction of the gate oxide interface where they become trapped in impurity sites. This means that positive charge buildup in PMOS devices is less severe than in NMOS, because the charges get trapped at the gate oxide interface. Thus, the charge buildup in PMOS devices is less effective in shifting the threshold voltage of the device [11]. Already it should be clear that the direction of the electric field in the gate oxide has a major effect on the radiation response of the device.

Conceptually, the radiation induced oxide charge buildup problems is a simple principle. It is only when one tries to quantify the details of the radiation response that one realizes the complexities involved in the radiation response of the MOS transistor. For example, the radiation response of a MOS transistor has a very complex time-dependant response which is not only important to understand the physics of the response, but also for the practical issues of testing, predicting and hardness assurance [12].

3. Overview Of The Mos Radiation Response

The MOS radiation response involves several different processes [13]. Each of these processes depends on time, temperature, applied field, process history, etc. as mentioned in the previous section. A basic illustration of the overall radiation response of the MOS transistor is shown in Fig. 2.

In Fig. 2 a positive bias voltage is applied to the gate terminal as in the case of NMOS. When ionizing radiation strikes the gate oxide, electrons are freed from the oxide molecules and are swept by the direction of the electric field towards the gate terminal. The free holes move in the direction of the substrate.

The four main processes involved in the radiation response of MOS devices are illustrated in Fig.2. First, the ionizing radiation acts with the gate oxide layer to produce electron-hole pairs [12, 13]. Some fraction of the electron-hole pairs recombine depending on the type of incident particle and the applied gate to substrate voltage, i.e. the electric field. The mass of the electron is much less than the mass of the hole, and is swept away very quickly in the direction of the gate terminal. The time for the electrons to be swept away is on the order of 1ps [13]. The much heavier holes that escape recombination remain near their point of origin. The number of these surviving holes determine the initial response of the device after a short pulse of radiation. The cause of the first process is the main motivation for design method described in the next section. The other processes will only be described briefly below. For a full review of these processes the reader is referred to [12, 13, 14, 15].

The second process in Fig. 2 is the slow transport of holes toward the oxide-silicon interface due to the presence of the electric field. It is this transport that explains the short term recovery of MOS devices [12]. When the holes reach the interface, process 3, they become trapped in impurity sites

and this is the main cause of the permanent threshold voltage shift in MOS devices.

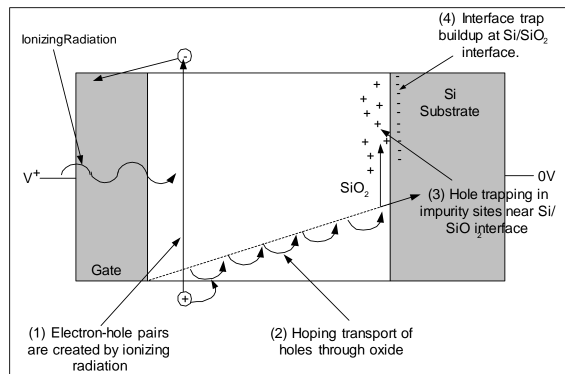

Fig. 2 The basic radiation effects in MOS transistors

The fourth process is the buildup of interface states in the substrate near the interface. A negative space charge region is created near the interface because of the positive charge buildup of process 3.

4. FPGA TID RESPONSE

A field-programmable gate array (FPGA) is a semiconductor device containing programmable logic components and programmable interconnects. It is the densest and most advanved programmable logic device. The FPGA allows a designer to implement large digital designs with relative ease at any time and location.

FPGA's typically consists of multiple copies of a basic programmable logic element (LE) or logic blocks. The logic element can implement a network of several logic gates that can then feed into 1 or two flip-flops. Logic elements are arranged in a column or matrix on the chip. To perform more complex operations, logic elements can be connected to other logic elements on the chip using a programmable interconnection network (Switching Architecture) [16].

A key aspect in the design of an FPGA is its switching architecture, which comprises the resources that are used to interconnect the device's logic blocks. There are three different FPGA switch technologies, SRAM, Flash and Antifuse. The differences in the radiation response in different FPGA technologies originate in the switches [17].

The key advantage of the Antifuse FPGA over other high-density programmable logic is the ionizing radiation tolerance of its programmable switch [17]. Substantial test data [17-19] indicates that an antifuse switch, either based on ONO (oxide-nitride-oxide) or MIM (metal-insulator-metal) technology, is immune to ionizing radiation, or total dose effects. Therefore, the total dose effects and hardening for an antifuse-based FPGA is determined by the technology on which its digital subsystem or logic part is based [20].

The SRAM FPGA's on the other hand consists of SRAM memory cells comprising the configuration memory of the device. Therefore, compared to an Antifuse FPGA, its sensitivity is increased because of the added effects on the SRAM switches. The TID sensitivity of Flash Based FPGA's will likely be determined by the floating gate switches [8, 21].

5. SWITHCED MODULAR REDUNDENCY

In this section we present the proposed Switched Modular Redundancy (SMR) method. The overall idea of the SMR method is as follows: A charged particle is accelerated in the presence of an electric field. If the field is removed, the charged particle becomes immobile. In process 1 of Fig 2, if we apply a zero bias to the gate terminal in the presence of ionizing radiation, both the free electrons and holes will remain near their point of origin, and therefore have a greater probability of recombination. The amount of threshold shift in MOS devices caused by ionizing radiation is strongly dependant on the bias voltage applied to the gate both during and after radiation [4]. Further, it has been reported that the trapped positive charge near the oxide-silicon interface anneal quickly when irradiated in an unbiased condition [4 - 7]. It is thus clear that the threshold voltage shift in MOS devices will be less severe for the gate terminal in an unbiased condition.

The fact that the rate of the threshold voltage shift in MOS devices is strongly dependant on the bias voltage applied to the gate terminal is a very important phenomena that can be exploited, since we have direct control and access to the voltage applied to the gate terminal.

If for example, two identical gates were under the influence of radiation and the gate voltage is alternated between the two, then the two gates should be able to withstand more total dose radiation than using only one gate. This redundancy could be used in a circuit to mitigate for total ionizing dose.

The more a MOS transistor is in use (i.e. switched ON), the more positive charge will be accumulated over time. This implies that gates that are longer in the ON state in a circuit will degrade faster than their idle (OFF) counter parts. Hence "ON" gates will suffer first and cause a circuit malfunction.

Consider Fig. 3. When input A is 0, Transistor T1 is in the ON state and T2 in the OFF state. Thus, in this situation, T1 is degrading in the influence of ionizing radiation, and T2 is annealing. This is illustrated in Table 1 with an X for degrading and √ for annealing.

Therefore, if we have a 50% duty cycle between the two transistors, the transistors should last longer than any other duty cycle. In a real digital circuit, this will not be the case.

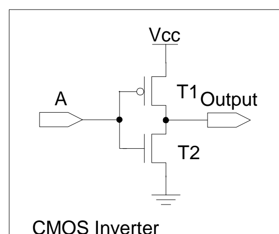

Fig. 3 CMOS Inverter Circuit

Table 1.

A	T1	T2
0	X	√
1	√	X

Hence, A might be 0 more often and the result is that T1 will degrade faster. The only requirement for this circuit to malfunction is for one transistor to fail.

A solution to this problem would be to add redundancy with an identical module in parallel. This is illustrated in Fig. 4.

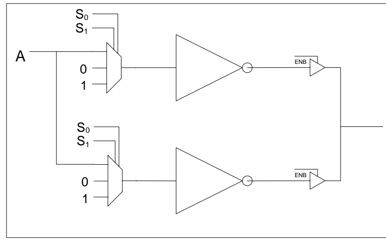

Fig. 4 CMOS Inverter with redundancy

The redundant group consists of only two components. While the one is in use, the other components inputs are varied between logic 1 and 0. Hence, while the one component is in use, the other component is given a time to anneal. The same method can be applied similarly to the other fundamental logic gates.

The SMR methodology would be to duplicate each gate in a circuit, then selectively only activating one gate at a time allowing the other to anneal during its off cycle. The SMR algorithm is code in the "C" language.

6 APPLYING THE SMR PRINCIPLE in FPGA's

The internal structure of an FPGA is very complicated and the design engineer has no access to individual gates, in fact, there are no fundamental gates in FPGA's [22]. The FPGA consists of logic blocks that are configured to implement a function that represents a fundamental gate. Even if we provided redundancy in the logic part (logic blocks) of the FPGA, we still would have a configuration memory that is constant for a particular FPGA implementation. For the SRAM based FPGA as well as the Flash-based FPGA, **switched** redundancy has to be provided in its configuration memory.

When the SRAM and Flash based FPGA is configured, the configuration memory determines the logic functionality of the FPGA. Hence, for a particular SRAM or Flash based FPGA implementation, the configuration memory is constant. Therefore, if we apply for example double redundancy to an SRAM or Flash based FPGA implementation, **we not only** duplicate the logic part of the FPGA, but as a consequence, we also duplicate the configuration memory.

The configuration memory controls the functionality of the FPGA, and it consists of either SRAM or Flash memory cells. However, even if we provided cycled redundancy in the logic part of the SRAM or Flash based FPGA, we still have a constant and static configuration memory that degrades under the influence if ionizing radiation. Thus, for the SRAM or Flash based FPGA, in order to mitigate for TID effects, we also have to provide the cycled redundancy to the configuration memory of the FPGA.

This reduces the problem of TID mitigation for the SRAM and Flash based FPGA to that of reconfigurable computing. This concept can be best explained by means of a diagram. Consider Fig. 5, which illustrates a simplified depiction of the interconnection between the configuration memory, and the logic part of the FPGA. If we apply redundancy to this system, the configuration memory will also be duplicated. Thus, for the SRAM FPGA, in order to implement cycled redundancy, we can reset one SRAM cell in the redundant group, while the original circuit is still configured with the other SRAM cell. This basically amounts to in-circuit reconfiguration.

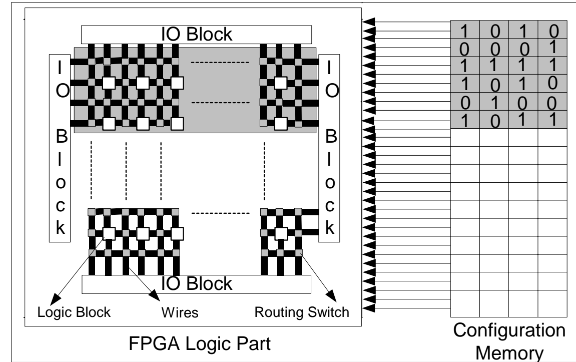

Fig. 5 Configuration memory and Logic Interconnection

FPGA's can be partially reconfigured to implement Dynamically loadable Hardware Plugin (DHP) modules. A tool called PARBIT has been developed that transforms FPGA configuration bitfiles to enable DHP modules.

With this tool it is possible to define a partial reconfigurable area inside the FPGA and download it into a specified region of the FPGA device [23]. Thus, the above theory can be physically implemented in FPGA's.

Another, and much simpler, way of solving this problem would be to provide no redundancy at all. We can simply load the same circuit into a different part of the configuration memory dynamically, as depicted in Fig. 6.

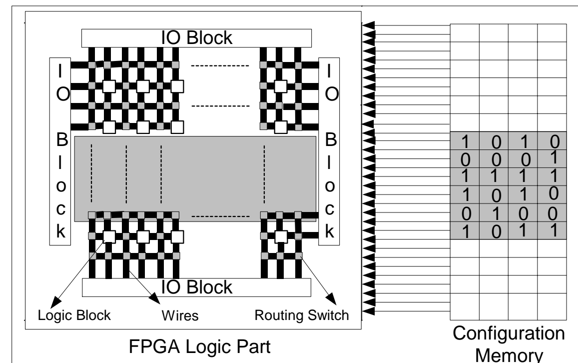

Fig. 6 Configuration memory swapping

After some time, the circuit will be reconfigured as in Fig. 5, and then back to that in Fig. 6, and so on. Thus, we define a partial reconfigurable area inside the FPGA and download it into a specified region of the FPGA device. In essence, configuration memory swapping is provided between the duplicated memory cells while the FPGA circuit is in operation.

7 EXPERIMENTAL RESULTS

In order to test the resting policy on SRAM FPGA's, the following setup was used. In the first instance, the FPGA was tested using normal operation and running a ring counter code (Case 1 in Fig. 7), while in the second case the FPGA was tested, also running the same code, however the power to the FPGA's were cycled (Case 2 in Fig. 7). The

FPGA's in case 1 of Fig. 7 started consuming more power supply current at about 15 krads and gradually increased in power supply. Intermittent IO errors started occurring at 18 kRad (Fig 8) until about 22 kRad when functional failure occurred. The FPGA's in case 2 of Fig. 7 also started consuming more power supply current, however at a slower rate as case 1. For case 2, the FPGA's were still functionally intact after 30 krads when the testing was stopped. This result shows that one can make use of system redundancy to increase the lifetime of SRAM FPGA's in space.

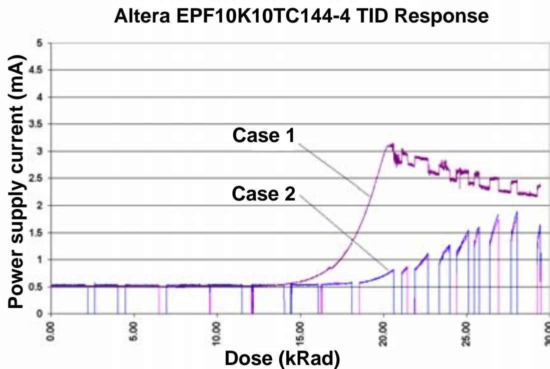

Fig. 7 Comparison between normal FPGA operation (Case 1) and FPGA power cycling (Case 2) for the Altera EPF10K10TC144-4 SRAM based FPGA.

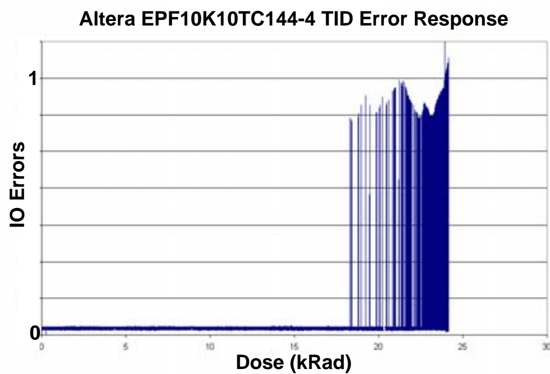

Fig. 8 FPGA IO errors for Fig. 7.

Further testing was performed on new FPGAs as follows: For the FPGA configured, but not clocked (case 2, Fig 9), the TID response is the same as with the normal operation (Case 1). Thus for case 2 of Fig. 9, the configuration memory is constant, but the switching matrix is not clocked. The zero clocking appears to have no effect. Thus, one could infer that the configuration memory plays an important role in the radiation response of the SRAM FPGA. This is because, although the FPGA is not clocked, the configuration memory is still constant, and degrades under the influence of ionizing radiation, as stated in the previous section. In case 3 of Fig 9, the FPGA is configured, and then tested in a radiation field as in case 1. However, after 2.5 krad, the configuration memory is reset, without switching the FPGA power off. For this case, the TID tolerance is much better than normal operation (Case 1). In fact, it is similar to when power was completely reset as in Fig. 7.

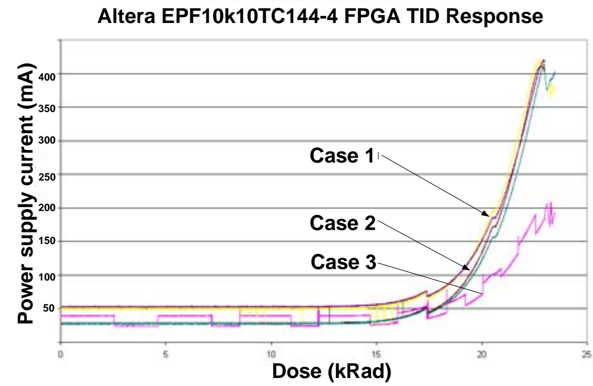

Fig. 9 Case 1: Normal operation as in case 1 above. Case 2: The FPGA is configured, but the clock signal is removed. Case 3: Normal operation, however the configuration memory were reset every 2.5 kRad.

Consider Fig. 10, after the FLEX 10K device has been configured, it was reconfigured in-circuit by loading to a different part of the configuration memory as described in the previous section (memory swapping). However, **the same IO ports were used during each reconfiguration**. Hence, only the internal FPGA core is different for each reconfiguration. This is represented by case 2 and 3. Reconfiguration requires less than 320 ms during system operation. The FPGA with normal operation (case 1) failed functionally at about 20 krad, whereas the reconfigured FPGA's failed functionally at about 33 krad. With the FPGA configuration memory swapping, a 65% increase in functional lifetime is observed.

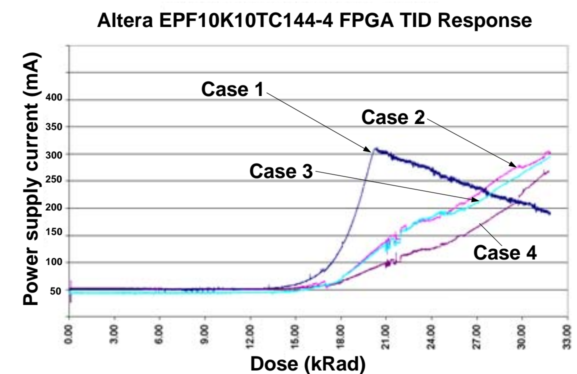

Fig. 10 Case 1: Normal Operation. Case 2, 3: Configuration memory is reset every half hour to a different part of the configuration memory. Case 4: Configuration memory is set to a different internal core as well as different IO ports.

In case 4 of Fig 10, the FPGA was reconfigured with both a different part of the configuration memory as well as different IO ports. Hence, a different internal core was used during each reconfiguration, as well as different IO ports. There seems to be an improved performance in case 4 compared to cases 2 and 3. However, with increasing absorbed dose, case 4's current soon increases and the FPGA failed functionally at 34 krad. The above results indicate that FPGA internal core redundancy provided TID mitigation, however, by also providing IO port redundancy does not further add to the functional lifetime of the FPGA. This does

not mean that the IO ports are immune against TID, however, the results does suggest that the IO ports have a higher tolerance to the radiation than the FPGA core for the measured absorbed dose. One can thus safely say that the FPGA core is the first and main source of the FPGA power supply current increase. Thus one can make use of the same IO ports for each reconfiguration and do not have to make changes to the PCB board.

8 Conclusions

We proposed a new design technique for TID mitigation in Field Programmable Gate Arrays. The method consists of applying Switched Modular Redundancy to the configuration memory in the FPGA. For devices which are subject to gate bias cycling, the maximum acceptable dose is higher than if the irradiation bias were applied continuously. By adding redundancy and applying a resting policy, one can significantly prolong the useful life of MOS components in space. It was shown experimentally that by applying FPGA system redundancy on a power cycling bases, the system lifetime is increased significantly. By resetting the configuration memory, the functional lifetime of the FPGA resembles that of power cycling. By applying redundancy in the configuration memory, the lifetime of the SRAM FPGA was increased in the presence of ionizing radiation. It was also shown that the IO ports do not contribute to the increase in power supply current and that the main cause of the increased current was due to the FPGA core.

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10 References

1. H.L. Huges and J.M. Benedetto, "Radiation Effects and Hardening of MOS Technology: Devices and Circuits", IEEE Transactions on Nuclear Science, Vol.50, No. 3, June 2003.
2. D. R. Alexander, "Design issues for radiation tolerant microcircuits for space", Notes of the Short Course of the IEEE Nuclear and Space Radiation Effects Conference, Indian Wells (California), July 1996, Section V.
3. S. E. Kerns, B. D. Shafer, L. R. Rockett et al., "The Design of Radiation-Hardened ICs for Space: A Compendium of Approaches", *Proceedings of the IEEE*, vol. 76, no. 11, November 1988, pp. 1470-1509.
4. T. Stanley, D. Neaman, P. Dressendorfer, J. Schwank, P. Winokur, M. Ackermann, K.Jungling, C. Hawkins, W. Grannemann, " The effect of operating frequency in the radiation induced buildup of trapped holes and interface states in MOS devices", IEEE Trans. Nucl. Sci. Vol NS-32, No. 6, Dec 1985.
5. T. Okabe, M. Kato, M. Katsueda, H. Kamimura, I. Takei, " High Frequency annealing effects on Ionizing Radiation response of MOSFET", IEEE Trans. On Nucl. Sci, Vol 37, No6, December 1990.
6. A. H. Johnston, "Annealing of total dose damage in the Z80 Microprocessor", IEEE Trans on Nucl Sci, Vol NS-30, No. 6, December 1983.
7. R.K. Freitag, C.M. Dozier, D.B. Brown, " Growth and annealing of trapped holes and interface states using time dependent biases", IEEE Trans on Nucl Sci, Vol. NS-34, No. 6, December 1987.
8. J.J. Wang, "Radiation effects in FPGA's", Actel Corporation, 11 May 2004.
9. Ed Smith "Effects of Realistic Satellite Shielding on SEE Rates", *IEEE Trans. on Nuclear Science*, vol 41, no. 6, pp. 0018-9499, Dec. 1994.
10. K.A. LaBel and M.M. Gates, "Single Event Effect Mitigation from the System Perspective", *IEEE Trans. on Nuclear Science*, vol 43, no. 2, pp. 654-660, Apr. 1996.
11. J.R. Srour, "Basic Mechanism of Radiation Effects on electronic Materials, Devices, and Integrated Circuits", Technical Report, Defense Nuclear Agency, Washington, 1982
12. T.R. Oldham, "Ionizing Radiation Effects in MOS Oxides", World Scientific Publishing, 1999.
13. T.R. Oldham, F.B. Mclean, H.E. Boesch, J.M. McGarrity, "An overview of radiation-induced interface traps in MOS structures", Semicond. Sci. Technol. 4 (1999) 986 – 999.
14. T.P. Ma, "Interface trap transformation in radiation or hot-electron damaged MOS structures", Semicond. Sci. Technol. 4 (1989) 1061 -1079.
15. J.R. Srour, C.J. Marshall, P.W Marshall, "Review of Displacement Damage Effects in Silicon Devices", IEEE Trans. Nucl. Sci., Vol. 50, No.3, June 2003.
16. J.O. Hamblen, M.D. Furman, "Rapid prototyping of digital systems", Kluwer Academic Publishers, 2003.
17. R. Katz, K. LaBel, J. Wang, B. Cronquist, R. Koga, S. Penzin, and G. Swift, "Radiation Effects on Current Field Programmable Technologies," *IEEE Trans. Nucl. Sci.* NS-44, 1945, (1997).
18. J. Wang, B. Cronquist, B. Sin, J. Moriarta, and Katz, "Antifuse FPGA for Space Applications," *RADECS 97 Data Workshop Record*, p. 11, (1997).
19. J. Wang, R. Katz, R. Koga, B. Cronquist, J. McCollum, and I. Kleyner, "Radiation Tests and Results of a Radiation Tolerant Antifuse FPGA, RT54SX," *RADECS 2000 Workshop Proceedings*, p. 253, (2000).
20. J.J Wang, B. Cronquist, J. McCollum, W. Parker, R. Katz, I. Kleyner, "Radiation tolerant Antifuse FPGA", Actel Corp., 2002
21. E.S. Snyder, P.J. McWhorter, T.A. Dellin, J.D. Sweetman, "Radiation response of Floating Gate EEPROM Memory Cells", IEEE Trans. On Nucl. Sci., Vol. 36, No. 6, December 1989.
22. J.O. Hamblen, M.D. Furman, "Rapid prototyping of digital systems", Kluwer Academic Publishers, 2003.
23. Edson L. Horta, John W. Lockwood, "PARBIT: A Tool to Transform Bitfiles to Implement Partial Reconfiguration of Field Programmable Gate Arrays (FPGA's)", Washington University, July 06, 2001.

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