Optical Polarization Mode Dispersion Compensator for 40 Gbit/s NRZ and RZ systems

R. Cigliutti[a], *Member, IEEE* ,A. Galtarossa[b], *Senior Member, IEEE*, M. Giltrelli[a], D. Grosso[b], A. W. R. Leitch[c], L. Palmieri[b], *Member, IEEE*, S. Santoni[a], L. Schenato[b], *Member, IEEE*, D. Waswa[c], *Member, OSA*

a Pirelli Labs, Viale Sarca 222, Milano, Italy
b Department of Information Engineering, University of Padova, Via Gradenigo 6/B, 35100, Padova, Italy,
Tel +39 049 8277660; Fax +39 049 8277699; email: andrea.galtarossa@dei.unipd.it
c Department of Physics, Nelson Mandela Metropolitan University, P.O. Box 77000, Port Elizabeth, 6031, South Africa,
Tel: +27 41 504 2141; Fax +27 41 504 2573; email: david.waswa@nmmu.ac.za

Abstract — Polarization Mode Dispersion (PMD) represents a major impairment for high bit rate systems resulting in pulse broadening and distortion and leading to system performance degradation if it is not handled properly. PMD is particularly difficult to assess because unlike chromatic dispersion, it varies stochastically in time. Basically, there are two different approaches to mitigate PMD effects: by deploying ultra-low PMD fibres or by using PMD compensators. While the former solution represents an option for new installations, the latter is the preferable solution for in-service systems. In this paper we present an optical PMD compensator able to compensate up to 25 ps of differential group delay in NRZ and RZ 40 Gbit/s systems.

Index Terms—Fibre optic, Polarization Mode Dispersion, Polarization Mode dispersion compensator.

I. INTRODUCTION

PMD compensation has been a matter of investigation of several papers in literature [1-4]. The proposed solutions belong basically to two large families: electronic compensators and optical compensators. Both PMD compensator schemes have advantages and disadvantages: electronic PMD compensators are usually simple to include in line-terminal, it is potentially low-cost, very fast, and FEC compatible but at the moment they can operate at a maximum of 10Gbit/s. Furthermore, they are strongly dependent on modulation formats and system margins, and they can compensate only one channel at a time.

Optical compensators are independent of the bit rate and of the modulation format and potentially they can compensate more channels simultaneously but their time response and feedback signal is not simple to process. In this paper we propose an optical PMD compensator. The device is simple to realize and easy to include in each EDFA module (distributed compensation) as well as a single-stage front-end compensator.

II. PMDC DESCRIPTION

The degree of polarization (DOP) reduction due to PMD effects in digital communication systems have been exhaustively discussed in literature [2, 5, 6]; by maintaining the DOP at a high level, the system is forced to reject PMD.

To understand how this device may compensate PMD, we may resort to the framework of principal state of polarization (PSP). As a matter of fact, to the first order the signal impinging on the PMDC can be decomposed in the two PSP's, which are delayed with respect to each other by an amount equal to the differential group delay (DGD). By maximizing the power transmitted by the polarizer, the control algorithm acts on the polarization controllers so as to align the input state of polarization (SOP) to the polarizer. In this way, the PSP that is carrying the largest amount of power is enhanced, while the other one is penalized; as a result, the quality of the signal is improved.

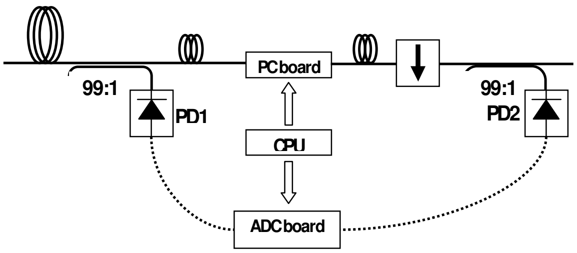

Fig. 1. PMD compensation system: functional block diagram (PC, polarization control; PD, photodiode; ADC, analogue to digital converter; CPU, central processing unit). The dotted and continuous lines represent electric busses and optical fibres respectively. Arrows are data/communication busses.

As an example, suppose that the PSP's are linearly polarized along the x- and y-axis, respectively; the former carries a power proportional to $(3/4)^{1/2}$, whereas the latter is proportional to 1/2. Consequently, the ratio between the two components is $3^{1/2}$ and the SOP is almost linear and at 30° with respect to the x-axis. A linear polarizer rotated at 30° would therefore attenuate the x-PSP by $(3/4)^{1/2}$ and the y-PSP by 1/2; the result is that the new ratio between the powers associated to the two PSP's is 3, which means that x-polarized PSP has been enhanced. Of course, the enhancement does not occur when the two PSP's carry the same power; however, this worst case situation is quite unlikely.

The adaptive Polarization Mode Dispersion Compensator (PMDC) proposed here is actually a first-order compensator, although it has some slightly beneficial effects also on higher-order PMD. As a consequence, it is designed to be used as a distributed compensator. In this respect, the strength of this PMDC is indeed its simplicity, which makes it easy and cheap to implement and integrate in EDFA modules.

Regarding the technical details, fig. 1 shows the functional block diagram of the PMD compensation system. A small part of the signal at the input of the polarization control (PC) board is coupled with photodiode PD1 to keep track of the input power level. This is required in order to allow the control algorithm to discern between power fluctuations due to PMD from those due to input power variations. The signal at the output of the PC board is passed through a polarizer and then partly coupled with photodiode PD2. The power level detected at PD2 is used as feedback signal and is maximized, so that the signal SOP just before the polarizer is aligned with the polarizer itself. The PC comprise of 4-axis voltage-controlled squeezers that induces polarization rotations in a controlled way. A personal computer runs the control algorithm and manages the communications with the PD's and the PC via RS232 and USB ports, respectively.

One of the most important parameters of a PMDC is the time response. In our preliminary setup the time response was mainly limited by the communication processes, which were implemented by means of high-level operating system calls. This bottleneck can be overcome by controlling the PMDC with dedicated electronics; in this case the ultimate limit to the response time would be the speed of the PC, which for our device is in the order of tens of microseconds per actuation. Because of this, in order to highlight the actual speed of the control algorithm, we measure the time in "steps", where each step is the time needed to change the voltage to one of the four squeezers.

III. PERFORMANCE TESTS

As a first action, tests have been performed to identify the effect of polarization scrambling on the PMD monitor signal, and to find the appropriate range of scrambling frequencies for which the compensator is still able to track and compensate for the SOP fluctuations.

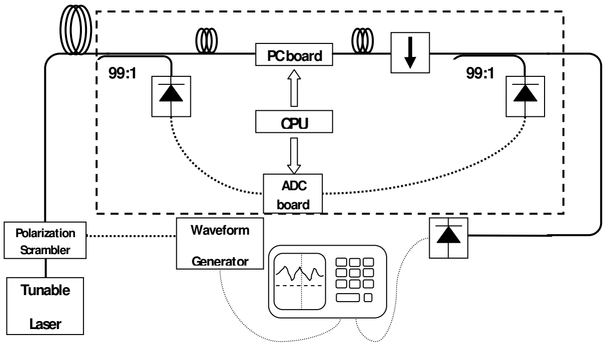

Fig. 2. Experimental setup for testing the system: functional block diagram.

Fig. 2 shows the experimental setup adopted during this characterization stage: a waveform generator is used to drive a polarization scrambler. The output signal detected by a photodiode with an oscilloscope is then used to track the response of the compensated system.

The waveform generator is used to provide ramp control signals with different periods, applied to one squeezer of a 4-axis polarization controller to vary the SOP of the input signal.

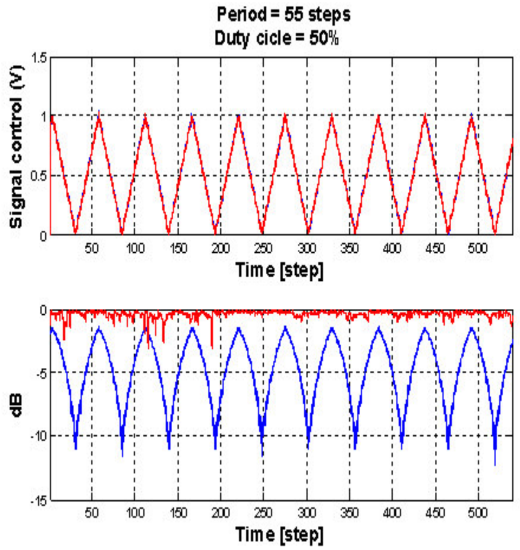

Fig. 3. Upper inset: Electrical signal used to control the scrambling. Lower inset: evolution of power of uncompensated signal (blue line) and of the compensated one (red line). The corresponding "scrambling" rate is approximately 3.6×10^{-1}dB/step.

The parameter of comparison to evaluate the performance of the compensator is represented by the capability of achieving (and maintaining) a certain power level in a certain time.

The choice of referring the performance of the device to the compensator time slot instead of an absolute time reference is motivated by the fact that, in this work, the effort has been mainly to optimize the control algorithm. Actually, the control algorithm is basically independent from the specific polarization controller hardware, so the speed issue can be easily overcome by adopting faster electronic and polarization controls.

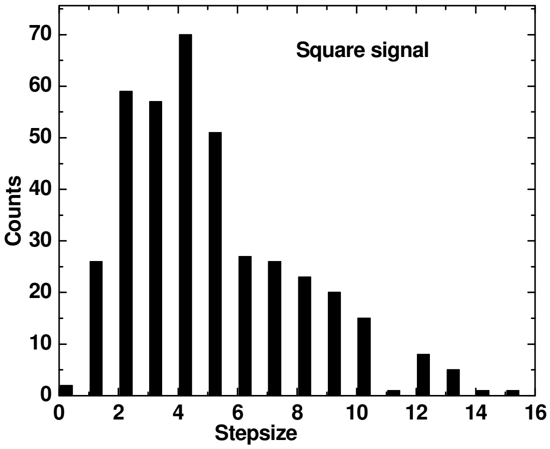

Fig. 4. Distribution of events with a maximum of 0.5 dB of PMDC excess loss for a square-wave signal applied to input SOP.

In fig. 3 the electric control signal that feeds the polarization scrambler is plotted in the upper inset, whereas in the lower inset the corresponding power fluctuation is represented when the compensator is not running (blue trace) and when it is working (red line).

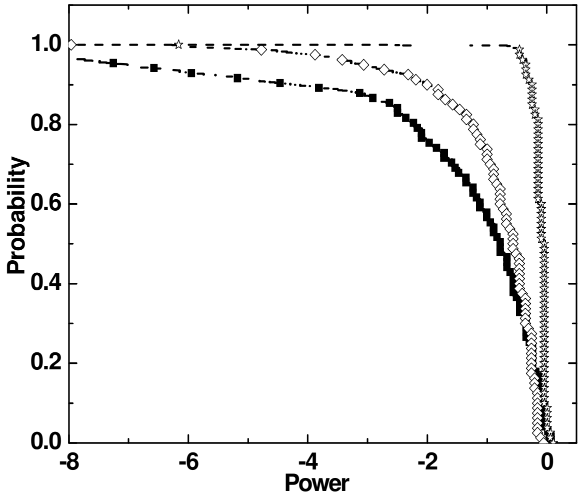

Fig. 5. CCDF vs PMDC insertion losses induced by a sine-wave variation of the input SOP (0.45 dB/step, 0.86 dB/step, 2.3 dB/step, respectively).

As one can see the power variation in absence of compensation may be as large as 10 dB.

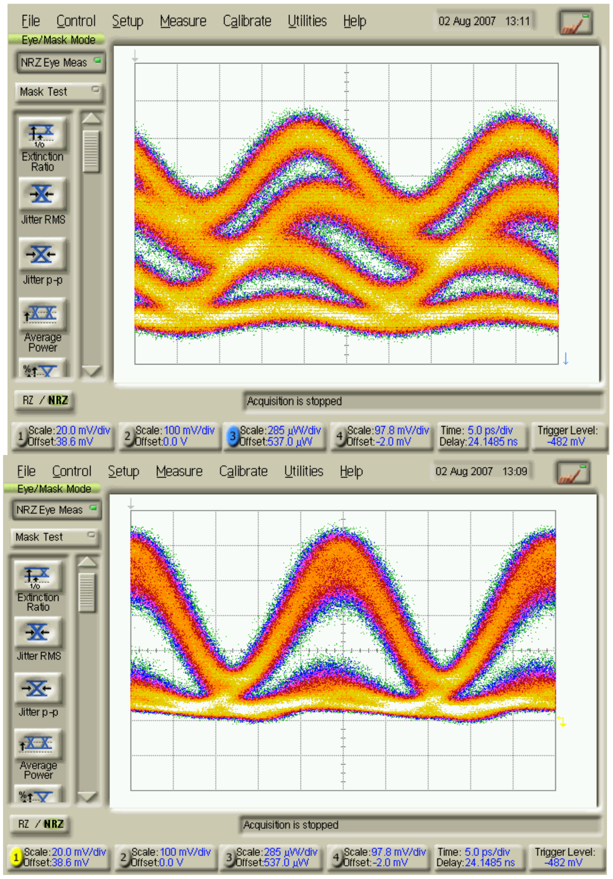

Fig. 6. Eye diagram for a DGD=20 ps and 40 Gbit/s RZ system: Upper inset PMDC input, lower inset PMDC output.

The compensator is able to compensate scrambling signals with period down to few tens of time slots. Moreover, by defining the "scrambling rate" as the rate of the maximum variation of the power of the uncompensated signal over half period of the scrambling signal, it follows that the compensator is able to effectively work up to 2.5 dB/step.

Other tests have been performed by using also a square-wave (to simulate sudden variations) and sine-wave (to simulate continuous slow changing drift). Fig. 4 shows the distribution of the steps necessary for the PMDC to lock a square-wave variation of the input SOP with 0.5 dB excess loss. The figure shows the number of steps necessary for the PMDC to align the SOP of the signal to the axis of the polarizer, validating the efficiency of the optimization algorithm.

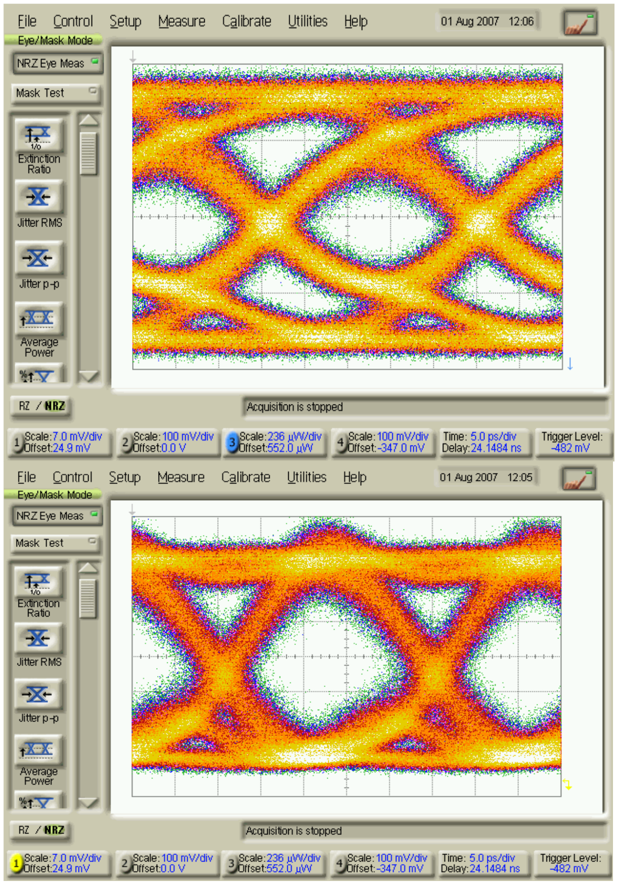

Fig. 7. Eye diagram for a DGD=20 ps and 40 Gbit/s NRZ system. Upper inset PMDC input, lower onset PMDC output.

In fig. 5 we report the Complementary Cumulative Distribution Function (CCDF) of the PMDC insertion loss when a sinusoidal electric signal is applied to the SOP of the input signal. From fig. 5 it is simple to infer that if we fix an upper limit of 1 dB to the PMDC induced insertion loss, we have a probability of 100% to achieve that target for a SOP variation of 0.45 dB/step and about 50% for a SOP variation of 2.3 dB/step.

Finally, we carried out extensive experimental testing on the PMDC by measuring the bit error rate (BER) for NRZ and RZ at 40 Gbit/s single-channel systems; PMD was generated by using a first order PMD Emulator (PMDE), tuning the DGD in the range 0-25 ps.

Figs. 6 and 7 show the eye diagrams for RZ and NRZ 40Gbit/s systems, respectively; the DGD generated by PMDE was 20 ps in both cases. Figs. 6 and 7 show the PMDC performances over signals degraded from a DGD as large as 20 ps with a power splitting ratio between PSP's of ≈4dB.

BER measurements are summarized in figs. 7 and 8. Three curves are reported in both figures: the upper (blue) line is the BER measurements without PMDC and with a DGD of 20 ps.

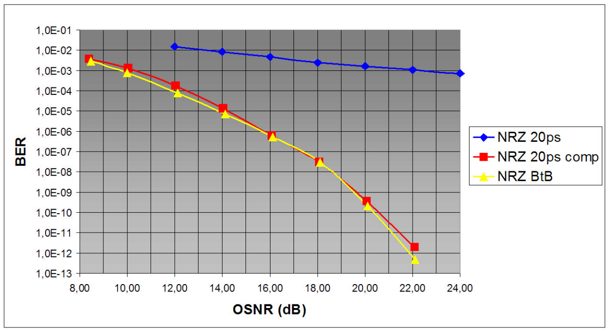

Fig. 8. BER test results on the NRZ system.

The two remaining lines correspond to the back-to-back BER measurements with DGD=0 (yellow line) and the BER result with a DGD = 20 ps compensated from the PMDC. Experimental results show that the PMDC allows one to recover both NRZ and RZ modulation formats, through a very good restoration of the transmitted signal, which is indicated from the overlapping between the back-to-back curves and the DGD compensated curves.

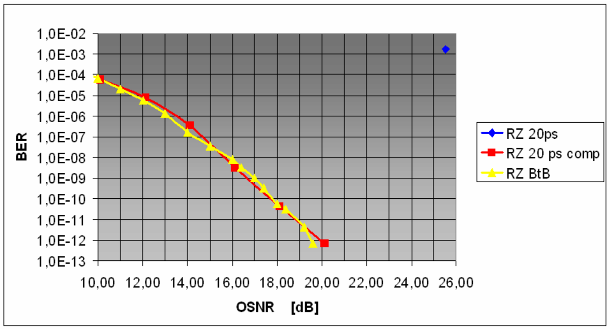

Fig. 9. BER test results on the RZ system.

IV. CONCLUSIONS

In this paper we have presented an optical first-order PMD compensator based on a DOP-feedback technique. We performed tests to determine the robustness of the device in presence of fast and wide variations of the input SOP. Finally we performed BER measurements on NRZ and RZ system at 40 Gbit/s to verify that both PMDC and control algorithm do not impact system transmission. All laboratory tests confirm the reliability of the device.

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Biographies

Roberto Cigliutti was born in Savona, Italy, in 1965. He received the degree (cum laude) in Electronic Engineering from the University of Genoa, Italy, in 1991. From 1991 to 1995, he worked with Marconi S.p.A., in Genoa, at the design of interfaces for SDH and ATM-PON applications. In 1995, he joined Pirelli Cables and Systems in Milan, where he was involved in CATV-Systems design and later was responsible of the Submarine Optical Repeater design team. From 1999 to 2003, he was head of the Transmission System Group inside the R&D of Pirelli Submarine Telecom Systems mainly focused on “repeatered” submarine optical links experiments and simulations. He has a patent on EDFA pumping scheme for submarine application, and some publications in long-haul transmission experiments. Since 2004 he was responsible of optical system applications studies for Pirelli Labs optical components. He is member of IEEE from 2000.

Andrea Galtarossa received the degree in Electronic Engineering from the University of Padova in 1984. In 1990 he joined the Department of Information Engineering (DEI), University of Padova, as assistant professor in Electromagnetic Fields (1990); he became associate professor in 1998 and full professor in 2006. His main research activities are: distributed measurements of polarization mode dispersion in fibres and optical components, PMD effects in high bit rate systems, PMD mitigation techniques. He is the inventor (or one of the inventors) of 5 US patents; he is co-author of about 100 regular and invited papers published in referred journals and conference proceedings. He is a senior member of IEEE, member of TPC of ECOC, associate editor of Optics Letters.

Massimo Giltrelli received the degree in Telecommunications Engineering from the University of Padova in 2002; in 2006 he received the Ph.D. in Electronic and Telecommunication Engineering form the same university in 2006. His main research activities during the Ph.D. were focused on Raman amplification, modulation formats and signal elaboration. In 2006 he joined Pirelli Labs (Milan, Italy), working on modelling and testing devices for PMD compensation. In 2008 he joined Telsey S.p.A. (Quinto di Treviso, Italy), where he is working on different research areas, including network architectures and devices.

Daniele Grosso: photo and biography not available.

Andrew Leitch: photo and biography not available.

Luca Palmieri was born in Belluno, Italy, in 1971. On 1996 he graduated with honours in Electronic Engineering at the University of Padova, Italy. He gained the PhD (2000); assistant professor at the University of Padova in 2003. Dr. Palmieri has participated and is participating in many national and international research projects (ACTS ESTHER, IST ATLAS, Italy-South Korea 2004/2006 and 2007/2009, IST NOBEL Phase II). He has authored and co-authored more than 30 scientific papers on international journals (four of which were invited) and almost as much on international congress proceedings. He holds 5 international patents.

Stefano Santoni: photo and biography not available

Luca Schenato was born in Verona, Italy, in 1979. He received the degree in Communication Engineering and the Ph.D. degree from the University of Padova, Padova, Italy, in 2003 and 2007, respectively. Since 2007 he is a research fellow at the University of Padova. He has co-authored more than 15 papers in international journals and almost as many in international conference proceedings. His research activity is mainly focused on polarization mode dispersion, PMD and birefringence measurements techniques, design of low-PMD optical fibres, nonlinear propagation in random birefringent fibres and slow light in optical fibre amplifiers. He is a member of IEEE.

David Waswa, a lecturer at Moi University, Kenya, is currently doing his doctoral studies at the Nelson Mandela Metropolitan University. His research interests are: Measurement and compensation of PMD and nonlinear distortion in the optical fibre. He is a member of OSA and SPIE journals