Stage 3 Performance of W-CDMA Cell Search for Various Chip Correlation Lengths

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***Abstract*--In W-CDMA radio access technology, 512 scrambling codes are employed to differentiate between the base stations. Unlike the CDMA2000, W-CDMA does not use absolute timing reference between its base stations. Therefore, the Mobile Station (MS) is given the daunting task of identifying the serving Base Station (BS) from a potential candidate set of 512 codes. Synchronization is achieved by intelligent de-scrambling of the codes at the receiver. Hence, the process where a mobile station searches for a serving base station is called Cell Search. It involves three stages. The first stage is timing recovery. The second stage is frame and scrambling code group identification. The third stage is scrambling code identification. This paper investigates the performance of the third stage of the cell search process for various chip correlation lengths. Moreover, a new algorithm that systematically correlates the received data sequence is proposed. The results show that the algorithm performs better than the existing algorithm when simulated with a flat Rayleigh fading channel, a Doppler frequency of 9.26 Hz and frequency offsets of up to 20 kHz.**

I. INTRODUCTION

There are two candidates for the third generation communication systems. These are CDMA2000 and W-CDMA. The former was designed based on its predecessor IS-95 Standard. W-CDMA was chosen as an evolutionary path for GSM (Global System for Mobile Communications). Though similar in many aspects, CDMA2000 and W-CDMA have a considerable difference in their synchronization techniques. This arises from the fact that W-CDMA is an asynchronous system while CDMA2000 is a synchronous one. Since asynchronous systems do not rely on an external timing reference, network deployment is much easier when compared to synchronous systems. To satisfy its network synchronization CDMA2000 uses an external timing reference (GPS) to accurately determine the transmission time of its base stations.

Contrary to CDMA2000, W-CDMA uses 512 scrambling codes to effectively separate the base stations from each other. Thus, the base stations operate on their own. Each base station transmits its data by scrambling it with one of the 512 codes. The mobile station is then faced with the task of identifying and locking to the transmitted scrambling code. However, base stations have to systematically transmit their scrambling codes to facilitate receiver operations. Studies on the progressive improvement to this systematic transmission of codes are given in [1-4]. These approaches are incorporated in the 3rd Generation Partnership Project (3GPP) Standard [5].

The 3GPP Standard classifies the 512 scrambling codes into 64 code groups [5]. Each code group then consists of 8 scrambling codes. The base station transmits specially designed codes to represent the code groups. To do this, the base station generates 16 Secondary Synchronization Codes (SSC), represented by C_i, where i = 1, 2,…16 specifies the SSC used [5]. To represent the 64 code groups, a set of sequences is transmitted in each frame with the order $(C_i, C_i,..., C_i)$ where C_i is chosen from the 16 SSCs. Each code word represents a specific scrambling code group. Moreover, the base station needs to send Primary Synchronization Codes (PSC) to assist in timing recovery at the receiver. The frame structure of a W-CDMA system is shown in Fig. 1. In a W-CDMA frame, there are 15 slots of 2560 chips each. There are 15 PSC sequences which are the same from slot to slot. The PSC and SSC are multiplexed at the first 256 chips of every slot in the frame. They are chosen to represent the code group of the transmitted scrambling code. The base station information is transmitted as a Common Pilot Channel (CPICH). The CPICH is scrambled by the cell specific scrambling code. There is only one CPICH per base station.

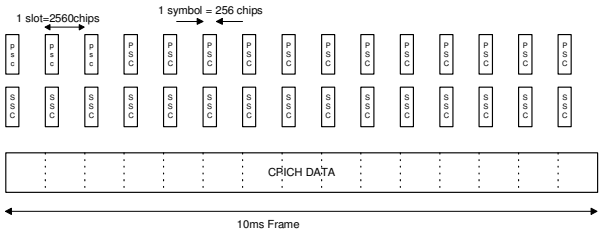

Fig. 1. Frame Structure of a W-CDMA System

The process of searching and synchronizing to a scrambling code is called cell search and consists of three stages [6]. Stage 1 recovers the timing information of the received code sequences by correlating it with the PSC sequence at 256 chip positions. After accumulating correlation values at 2560 chip positions (one slot), the chip position with a maximum correlation value is selected as a possible position for the start of slot. In Stage 2, the received

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signal is correlated with all the 16 SSC sequences at 256 chip positions of every slot position. The results are accumulated over one frame (15 slots). The SSC sequences with the highest correlation values are then selected for each of the 15 slots. The sequence of the selected SSCs is then correlated with each of the 15 cyclic shifts of the 64 code words. The codeword and the cyclic shift that maximizes the correlation value are then chosen as a possible scrambling code group and start of frame respectively.

Since each of the code words consist of 8 scrambling codes, Stage 3 continues the cell search process by correlating the received signal with each of the scrambling codes within the selected code group. The maximum correlation value gives the transmitted scrambling code. This process is studied in detail in Section II.

One of the many challenges encountered in a cell search receiver design is frequency offset. This arises when the local oscillator at the receiver oscillates at a different frequency to that of the transmitter. The difference in frequency is seen as a frequency offset by the receiver and is the major cause of receiver communications failure [7]. In a W-CDMA system, the frequency offset is estimated to be in the range 6-26 kHz [6]. Several papers have tried to mitigate this problem [6, 8]. This paper investigates the effect of using various chip correlation lengths on the performance of cell search. Results are obtained by simulating Stage 3 of the cell search process.

The paper is organised as follows. Section II presents the system model used for simulating the stage 3 of the cell search. A new algorithm that exploits parallel correlation of chip sequences is proposed in Section III. Simulation results are presented in Section IV. Finally, the conclusion is presented in Section V.

II. SYSTEM DESCRIPTION

This section presents the system description of the model used in this paper. The scrambling codes are generated using a Gold code generator of length 18 [5]. Out of 2^{18}-1 possible codes, only 512 codes are used to differentiate between the base stations. The codes are then truncated to satisfy the 10ms frame constraint of a W-CDMA system. Thus, 38400 chips are generated. Gold codes have very good autocorrelation properties [5].

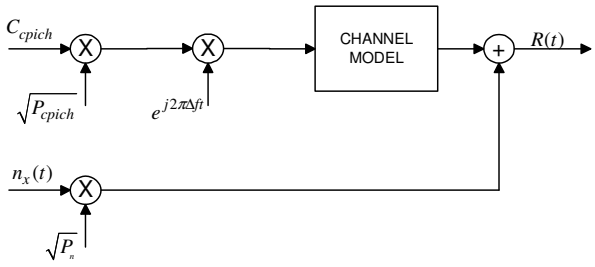

Fig. 2. Model used to study Stage 3 performance

Fig. 2 shows the model used to determine the performance of Stage 3 of the cell search process [6]. C_{cpich} represents the base station data that is scrambled with the scrambling code of the base station. P_{cpich} is the power of the transmitted base station data. $n_x(t)$ is the system noise and is modelled as Additive White Gaussian Noise (AWGN). P_n is the noise power. Δf represents the frequency offset at the receiver. $e^{j2\pi\Delta ft}$ is used to model the effect of frequency offset on the transmitted data. A flat Rayleigh fading channel is assumed [9]. *R(t)* represents the received signal and is fed into a Stage 3 synchronizing system. For a flat fading channel envelope $\alpha(t)$, the received signal *R(t)* can be written as

$$R(t) = \sqrt{P_{cpich}}\, C_{cpich}(t)\, e^{j2\pi\Delta ft}\, \alpha(t) + \sqrt{P_n}\, n_x(t) \qquad (1)$$

The receiver assumes the slot timing, the frame timing and the scrambling code group are already known. Moreover, discrete samples at intervals of the chip duration are used. The conventional way of detecting the scrambling code is presented below.

The Stage 3 synchronizing system uses the Gold code generator to generate all the 8 scrambling codes within the detected scrambling code group (one group is selected from a possible of 64 code groups). The received signal *R(t)* is then correlated with each of the *k* scrambling codes. The correlation can be written as

$$D(q,k) = \sum_{j=1}^{256/M} \left| \sum_{i=1}^{M} R\left(i + M(j-1) + T(q-1)\right) C^{(k)}\left(i + M(j-1) + T(q-1)\right) \right|^2 \qquad (2)$$

where *D(q,k)* is the correlation value of the received signal with each of the q^{th} symbol of the *k* locally generated scrambling codes $C^{(k)}(\bullet)$, where *k = 1,2…8* and *q* = 1,2,…,150 (denotes the number of symbols in one frame). Moreover the partial correlation length is denoted by *M*. The symbol duration in chips is *T* (*T* = 256). Most authors limit the partial correlation length to 64 chips if the frequency offset is 20 kHz or 256 chips if the frequency offset is less than 200 Hz. This paper investigates the effects of various chip correlation lengths (*M*) on the performance of Stage 3.

The most likely transmitted scrambling code is identified as follows. Let $\Lambda(k)$, *k* as defined above, represent a counter at the mobile station that keeps track of votes for the eight scrambling codes. For example, $\Lambda(3)$ will represent the number of times (of possible 150 symbols) the scrambling code number *k* = 3 has achieved a high correlation value in (2). The total sum of votes in the counters is equal to the number of symbols in the frames considered (i.e. 150 symbols for one frame). This can be written as

$$\sum_{k=1}^{8} \Lambda(k) = 150 \times (number\ of\ frames) \qquad (3)$$

After accumulating votes for all the symbols, majority voting is done to choose the most likely transmitted code. This is verified by comparing the chosen vote with a threshold T_h . Threshold setting is discussed in [6]. For a false detection probability of 10^{-4} and for a synchronization time of one frame, the threshold is calculated to be T_h = 38 [6]. The process stops if and only if the majority vote is greater than T_h .

III. PROPOSED ALGORITHM

The process described in Section II follows a conventional way of exploiting the correlation length for high frequency offsets. To this end, for an offset of 20 kHz, the 256 chip symbol is divided into four 64 chip divisions. The outputs of these correlations are then non-coherently combined [6]. This paper extends this work for the correlation lengths M = 16, 32, 128, 256 chips.

The shortcoming of the above method lies in its inability to determine the performance given a correlation length different from M = 16, 32, 64, 128, 256 chips. The proposed algorithm improves on the above problem. It investigates the possibility of using correlation lengths that lie in between the values specified above. To do this, the 256 chip correlation interval is exploited in a different way. Two parallel correlators are employed. Fig. 3 illustrates the use of this method for $M \in (64,85]$ [1]. The 256 chip symbol is divided into four correlation intervals. Each correlation interval is of length M (M does not necessarily has to be divisible by 256). This results in an overlap (shown shaded).

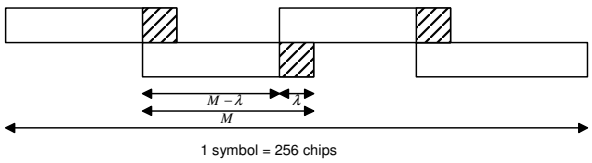

Fig. 3. Symbol exploitation of the proposed algorithm

The receiver systematically calculates the starting position for the next correlation interval. For this, the overlapping interval (in chips) has to be subtracted from M. The overlapping interval λ is calculated (in chips)

$$\lambda = \left\lceil \frac{M * \left\lceil \frac{256}{M} \right\rceil - 256}{\left\lfloor \frac{256}{M} \right\rfloor} \right\rceil \tag{4}$$

where $\lceil \bullet \rceil$ denotes the closest upper integer value of the fraction and $\lfloor \bullet \rfloor$ denotes the closest lower integer value of the fraction. The correlation of the received signal with the scrambling codes in (1) can now be modified to include this overlapping interval length.

$$D(q,k) = \sum_{j=1}^{256/M} \left| \sum_{i=1}^{M} R\left(i+(M-\lambda)(j-1)+T(q-1)\right) C^{(k)}\left(i+(M-\lambda)(j-1)+T(q-1)\right) \right|^2 \tag{5}$$

The rest of the procedure is the same as outlined in Section II. The contribution of the new algorithm is to reconfigure the partial correlation structure of every received symbol with a view to investigating the possibility of using a wide variety of M depending upon the frequency offset.

IV. SIMULATION RESULTS

Performance evaluation was done through simulation. Since the focus of this paper is on Stage 3 of the cell search process, the PSC and SSC codes are not included in the base station data. Hence, the base station data is generated using the all 1's CPICH data which is then scrambled by a cell specific scrambling code. The cell-specific scrambling code is generated using the Gold code generator shown in [5].

The effects of frequency offset and channel coefficients are then included in the BS data. This paper considers the frequency offset to be in the range 5 - 20 kHz. The filtered white Gaussian noise model [9] is used to derive the channel coefficients of a flat fading channel with a Doppler frequency of 9.26 Hz and with a filter length of 127. The noise is modelled as AWGN. The received data is then passed through the Stage 3 synchronization algorithm described in Sections II-III. The probability of miss detection is used as a performance measure. It is defined as the probability of the algorithm failing to detect the transmitted scrambling code from the received signal [6]. It is assumed that the algorithm knows the start of the slot, the start of the frame and the scrambling code group of the transmitted signal. Monte Carlo simulations are used with 1000 iterations for each probability of miss detection.

Fig. 4 shows the performance of Stage 3 for the conventional and the proposed algorithms. The frequency offset is 20 kHz. Different values of correlation length are considered. M = 64 gives an optimum performance with the conventional system. The performance degrades for higher values of M due to high value of frequency offset. An improvement is recorded when considering lesser signal to noise ratios. The proposed algorithm, however, performs better that the conventional one for values of M in the range 16 to 128. The performance degrades for values of M between 128 and 256. Optimum performance is achieved for values of M in the range 32 to 64. When M = 16, 32, 64,128 and 256 chips, the proposed algorithm reduces to the conventional one. This is because the overlapping length λ is zero in (4) for the above values of M. The proposed algorithm is therefore a modified version of the algorithm presented in Section II.

[1] For $M \in (64,85]$ there can only be four partial correlations within 256 chips. For example if M=50, 6 partial correlations are performed for an overlap to take place. However, the algorithm dynamically chooses the number of partial correlations within the symbol period.

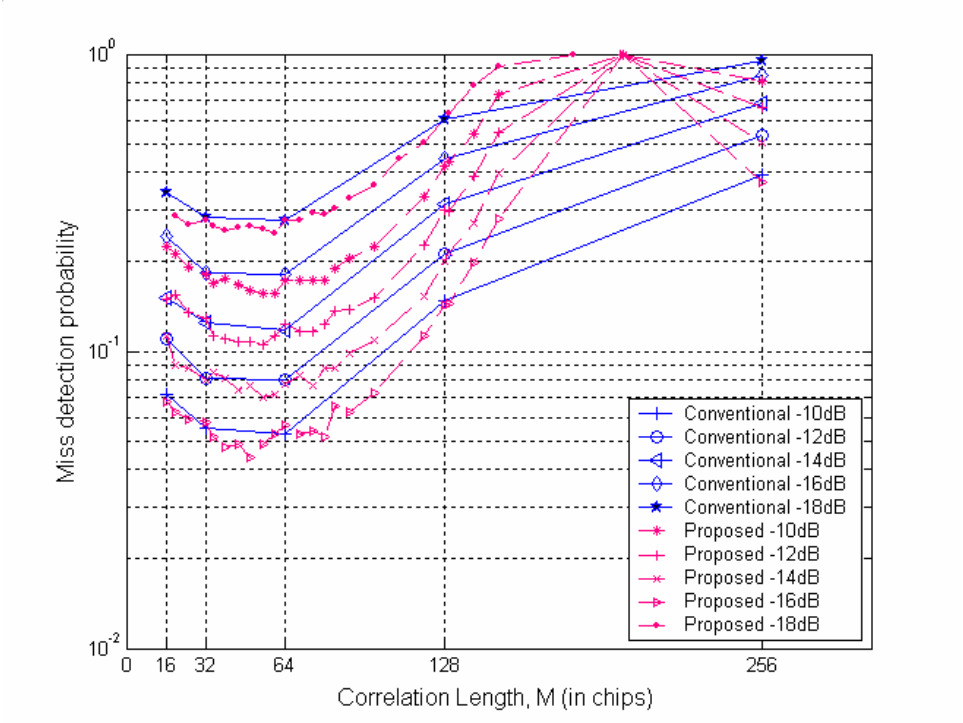

Fig. 4. Performance of Stage 3 (Frequency Offset = 20 kHz)

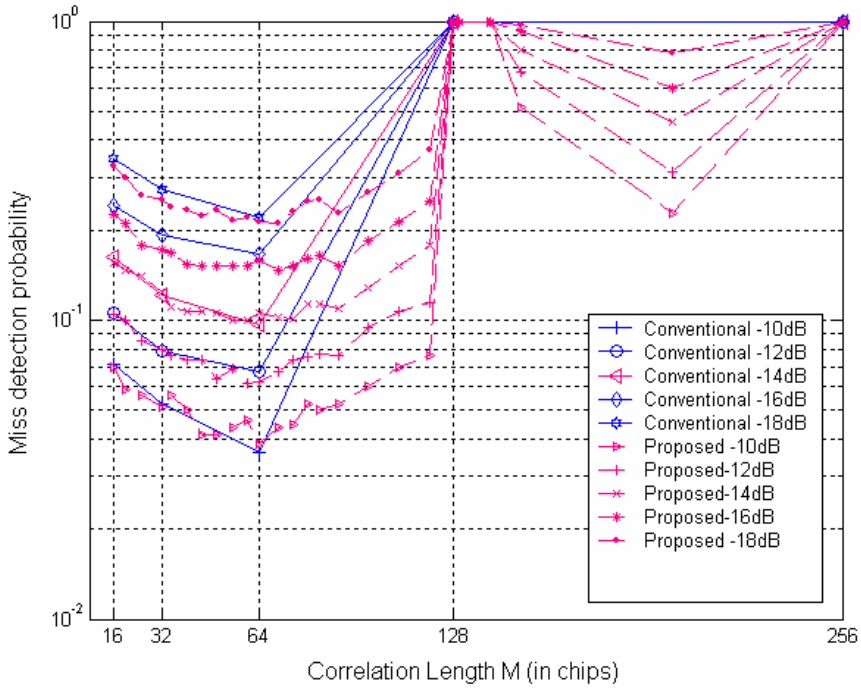

Fig. 5. Performance of Stage 3 (Frequency Offset =15 kHz)

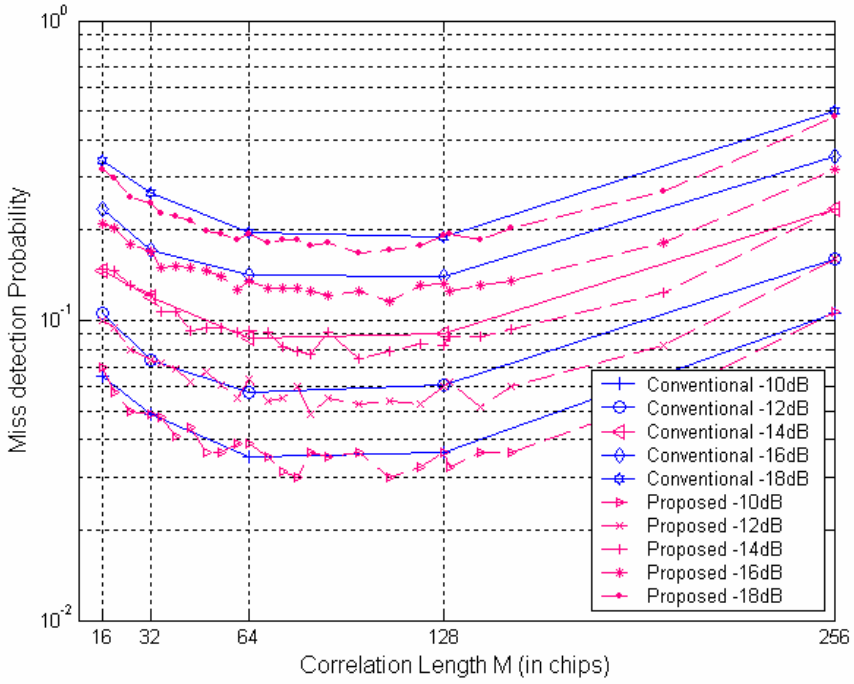

Fig. 6. Performance of Stage 3 (Frequency Offset = 10 kHz)

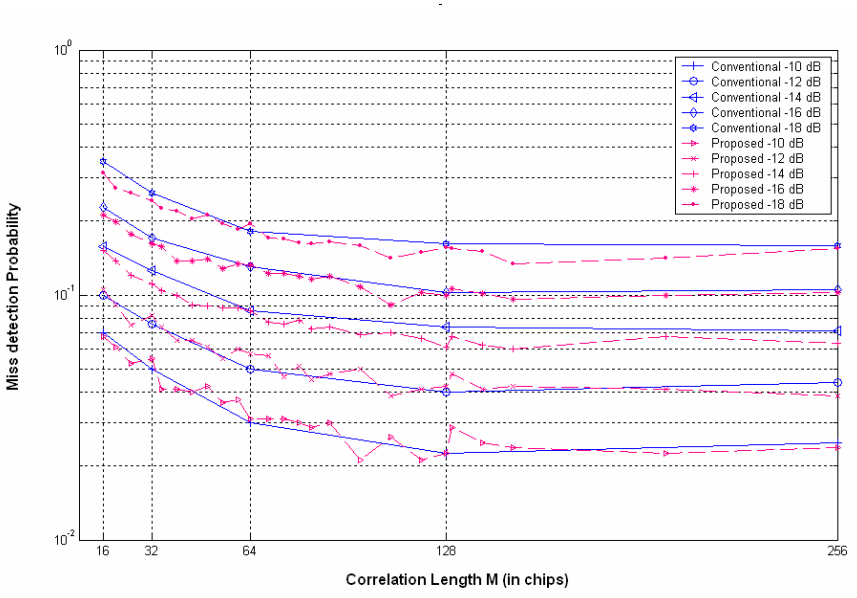

Fig. 7. Performance of Stage 3. (Frequency Offset = 5 kHz)

Fig. 5 records the worst performance for both the proposed and the conventional algorithms at correlation lengths of 128 and 256 chips. At these points, there is a complete phase rotation of the received signal due to the 15 kHz frequency offset. The proposed algorithm is shown to have a better performance for most values of *M*. Both algorithms tend to have similar optimum performance when a 15 kHz frequency offset is considered.

Fig. 6 and Fig. 7 show the Stage 3 performance when 10 kHz and 5 kHz frequency offsets are considered respectively. The performance of M = 256 chips shows an improvement in both cases. This is because the received signal suffers less distortion at these frequency offsets. Moreover, an improvement is shown as the signal to noise ratio decreases. The proposed algorithm is seen to have improved the optimum performance for values of *M* between 64 and 128 chips in Fig. 6

V. CONCLUSION

This paper addressed the procedures involved in a W-CDMA cell search process. The conventional approach is discussed and its performance is extended for various values of the correlation length. It is shown that for this approach, $M = 64$ chips gives the optimum detection performance at a frequency offset of 20 kHz. Moreover, a new algorithm that exploits the partial correlation interval while maintaining the symbol duration is proposed. Its performance is evaluated and is shown to improve on the conventional algorithm.

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